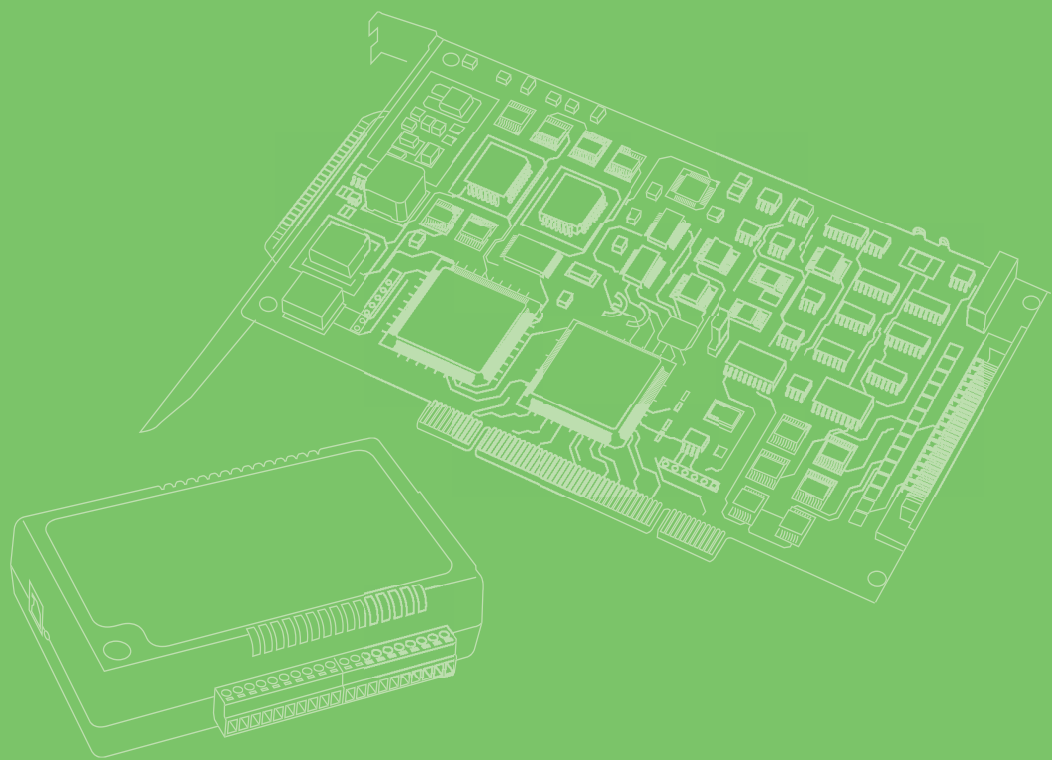


User Manual



iDAQ-784

4-ch, 32-bit, Encoder Counter/
Timer Industrial DAQ Modules

ADVANTECH

Enabling an Intelligent Planet

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Product Warranty (2 years)

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This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

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If you believe your product is defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This type of cable is available from Advantech. Please contact your local supplier for ordering information.

Test conditions for passing also include the equipment being operated within an industrial enclosure. In order to protect the product from damage caused by electrostatic discharge (ESD) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class A

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference. In such cases, users are required to correct the interference at their own expense.

警告使用者

這是甲類測試產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策。

Technical Support and Assistance

1. Visit the Advantech website at www.advantech.com/support to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
 - Product name and serial number
 - Description of your peripheral attachments
 - Description of your software (operating system, version, application software, etc.)
 - A complete description of the problem
 - The exact wording of any error messages

Warnings, Cautions, and Notes

Warning! Warnings indicate conditions that if not observed can cause personal injury!



Caution! Cautions are included to help prevent hardware damage and data losses. For example,



“Batteries are at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.”

Note! Notes provide additional optional information.



Document Feedback

To assist us with improving this manual, we welcome all comments and constructive criticism. Please send all such feedback in writing to support@advantech.com.

Packing List

Before system installation, check that the items listed below are included and in good condition. If any item does not accord with the list, contact your dealer immediately.

- iDAQ-784
 - iDAQ-784 x 1
 - Startup Manual x 1

Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect the equipment from all power outlets before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergents.
4. For pluggable equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect the equipment from humidity.
6. Place the equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. Do not cover the openings.
8. Ensure that the voltage of the power source is correct before connecting the equipment to a power outlet.
9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.

10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage from transient overvoltage.
12. Never pour liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If any of the following occurs, have the equipment checked by service personnel:
 - The power cord or plug is damaged.
 - Liquid has penetrated the equipment.
 - The equipment has been exposed to moisture.
 - The equipment is malfunctioning, or does not operate according to the user manual.
 - The equipment has been dropped and damaged.
 - The equipment show obvious signs of breakage.
15. Do not leave the equipment in an environment with a storage temperature of below $-20\text{ }^{\circ}\text{C}$ ($-4\text{ }^{\circ}\text{F}$) or above $60\text{ }^{\circ}\text{C}$ ($140\text{ }^{\circ}\text{F}$) as this may damage the components. The equipment should be kept in a controlled environment.
16. **CAUTION:** Batteries are at risk of exploding if incorrectly replaced. Replace only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.
17. In accordance with IEC 704-1:1982 specifications, the sound pressure level at the operator's position does not exceed 70 dB (A).

DISCLAIMER: These instructions are provided according to IEC 704-1 standards. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Wichtige Sicherheitshinweise

1. Lisez attentivement ces consignes de sécurité.
2. Gardez ce manuel pour référence future.
3. Déconnectez cet équipement de toute prise secteur avant de le nettoyer. Utilisez un chiffon humide. Ne pas utiliser de liquide ou de sprays détergents pour le nettoyage.
4. La prise de courant doit être située près de l'équipement et doit être facilement accessible.
5. Gardez cet équipement à l'abri de l'humidité.
6. La chute de l'équipement pouvant l'endommager, celui-ci doit être installé sur une surface stable.
7. Les ouvertures du boîtier sont nécessaires au refroidissement de l'appareil. Veillez à protéger l'appareil contre la surchauffe. **NE PAS COUVRIR LES OUVERTURES.**
8. Assurez-vous que la tension de la source d'alimentation est correcte avant de brancher l'appareil à la prise de courant.
9. Placez le cordon d'alimentation de manière à éviter que des personnes marchent dessus. Veillez à ce qu'aucun objet ne soit placé sur le cordon d'alimentation.
10. Tous les conseils et avertissements concernant ce matériel et son utilisation doivent être lus et compris.
11. Si l'appareil n'est pas utilisé pendant une longue période, débranchez-le de la source d'alimentation pour éviter les dommages causés par des surtensions transitoires.
12. Ne jamais verser de liquide dans une ouverture. Cela peut provoquer un incendie ou un choc électrique.
13. Ne jamais ouvrir l'équipement. Pour des raisons de sécurité, l'équipement ne peut être ouvert que par du personnel qualifié.
14. Si l'une des situations suivantes se présente, faites vérifier le matériel par le personnel de service:
 - Le cordon d'alimentation ou la prise est endommagé.
 - Du liquide a pénétré dans l'appareil.
 - L'équipement a été exposé à l'humidité.
 - L'équipement ne fonctionne pas bien, ou vous ne pouvez pas le faire fonctionner selon le manuel d'utilisation.
 - L'appareil est tombé et est endommagé.
 - L'équipement présente des signes évidents de casse.
15. Ne pas laisser ce matériel dans un environnement où la température de stockage peut descendre en dessous de -20°C (-4°F) ou être supérieure à 60°C (140°F). Ceci pourrait endommager l'équipement. L'équipement doit être maintenu dans un environnement contrôlé.
16. **ATTENTION: RISQUE D'EXPLOSION SI LA BATTERIE EST REMPLACÉE DE MANIÈRE INCORRECTE.** Remplacer uniquement avec un modèle recommandé par le fabricant, et éliminer les piles usagées selon les instructions du fabricant.
17. Conformément à la norme CEI 704-1:1982, l'opérateur ne doit pas expérimenter un niveau sonore supérieur à 70 dB (A).
18. **AVERTISSEMENT:** Ces consignes suivent la norme CEI 704-1. Advantech décline toute responsabilité concernant l'exactitude des déclarations contenues dans ce document.

Safety Precautions - Static Electricity/Précautions de sécurité - électricité statique

Follow these simple precautions to protect yourself from harm and the products from damage.

Suivez ces précautions simples pour vous protéger contre les blessures et les dommages aux produits.

- To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards while the PC is powered on.
Pour éviter les chocs électriques, assurez-vous de débrancher le boîtier de l'ordinateur avant de procéder manuellement. Lorsque l'ordinateur est allumé, ne touchez pas les composants de la carte CPU ou d'autres cartes.
- Disconnect the power before making any configuration changes. A sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.
Déconnectez l'alimentation avant de modifier la configuration. Une panne soudaine après le raccordement ou l'installation d'une carte peut endommager les composants électroniques sensibles.

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Chapter 1

Start Using iDAQ-784

1.1 Product Overview

This chapter provides an overview of Advantech industrial data acquisition (iDAQ) module for iDAQ-784, ranging the product lineups, features, driver, utility and accessories. The iDAQ-784 is a 4-ch encoder & counter iDAQ module. It includes four 32-bit encoder counters with programmable trigger output (preload FIFO) for position comparison which is suitable for motor control and position monitoring applications.

All of the iDAQ modules could be used in all kinds of iDAQ chassis. In the following sections, the detailed use instruction and functions will be described.

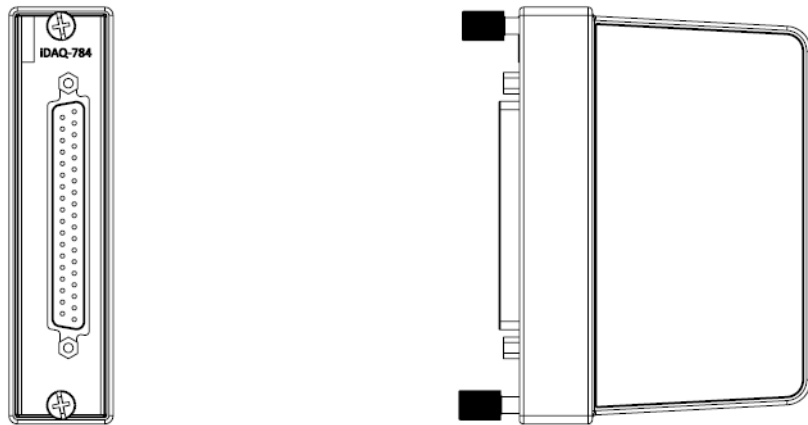


Figure 1.1 iDAQ-784

1.2 Product Features

1.2.1 Power Input

The power input of all the iDAQ I/O modules comes from iDAQ chassis through the DB 15-pin connector. The iDAQ I/O modules would be powered on when the power of iDAQ chassis is connected.

1.2.2 BoardID

A board ID can be assigned to the iDAQ chassis by the rotary switch and slot number. The board ID will be shown in the software and can be used to distinguish modules. The number shown around the rotary switch is in hexadecimal format. For example, "A" represent 10 in decimal format, and "F" represents 15 in decimal format. The number assigned to each iDAQ module follows a rule combining the ChassisID and slot number.

1.2.3 Plug and Play Device

iDAQ modules are hot-swappable in iDAQ chassis. The modules are recognized instantly in the software when they're plugged into the iDAQ slots, the same when they are unplugged. Therefore, it's strongly recommended not to perform this while the system is in acquisition mode - the system should be in idle mode.

1.3 Driver Installation

The driver package can be found on the Advantech Support Portal (<https://www.advantech.com/support>). Search for iDAQ on the support portal, then the corre-

sponded driver/SDK package can be found. You'll get the XNavi installer after the download session finishes.

Execute the installer, then it will guide you through the session. You can choose the device and software components you'd like to install in the system (figure 1.2). After the selection, click on "start" to begin the installation.

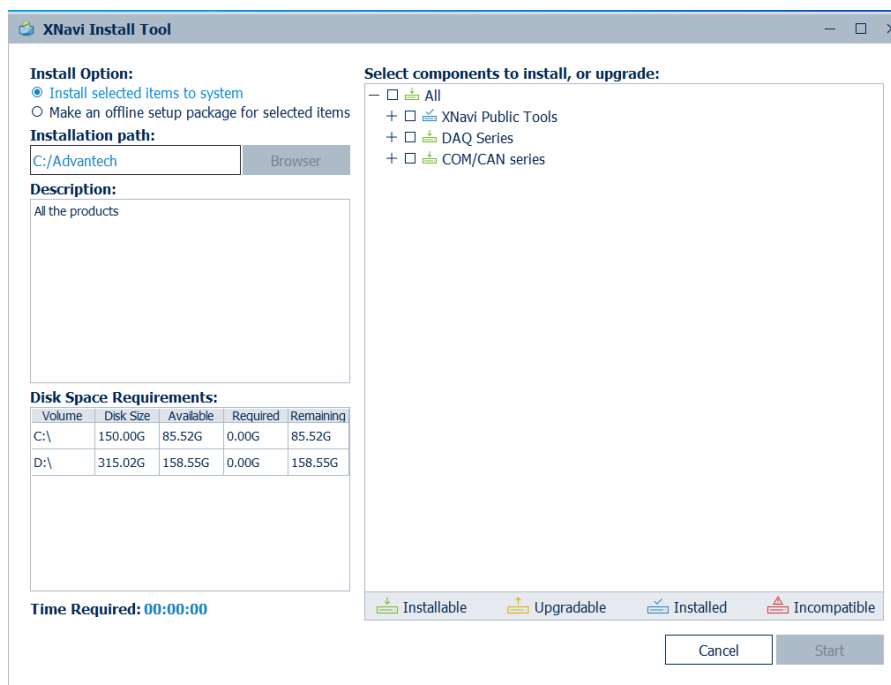


Figure 1.2 XNavi Installer

1.4 Software Utility

Advantech offers device drivers, SDKs, third-party driver support and application software to help fully exploit the functions of your iDAQ system. All these software packages are available on the Advantech website: <http://www.advantech.com/>.

The Advantech Navigator is a utility that allows you to set up, configure and test your device, and later stores your settings in a proprietary database.

1. To set up the I/O device for your card, first run the Advantech Navigator program (by accessing Start/Programs/Advantech Automation/DAQNavi/Advantech Navigator). The settings can also be saved to to your hard drive.
2. You can view the device(s) already installed on your system (if any) on the Installed Device tree view. If the software and hardware installation are completed, you will see iDAQ modules in the Installed Devices list.

1.5 Software Development Using DAQNavi SDK

DAQNavi SDK is the software development kit for programming applications with Advantech DAQ products. The necessary runtime DLL, header files, software manual and tutorial videos could be installed via XNavi installer. They can be found under C:\Advantech\DAQNavi (default directory) after the finishing the installation.

1.6 FPGA Code Update

The FPGA can also be updated via the interface in Navigator. However, it isn't normal to make an FPGA update. Advantech strongly suggests you to consult your technical support before starting an FPGA update process.

1.7 Ordering Information

IDAQ-784-A 4-ch, 32-bit, Encoder Counter/Timer Industrial DAQ Modules

1.8 Accessories

PCL-10137-1E DB-37 Shielded Cable, 1m

PCL-10137-2E DB-37 Shielded Cable, 2m

PCL-10137-3E DB-37 Shielded Cable, 3m

ADAM-3937-BE DB-37 Wiring Terminal, DIN-rail Mount

Chapter 2

Installation and Field
Application

2.1 Installation

This section provides guides from module installation to signal wiring for the iDAQ modules.

Below are the steps to insert the iDAQ modules into the iDAQ chassis.

1. Insert the module and follow the guide rail to the end.
2. Fix the two screws tight onto the chassis.

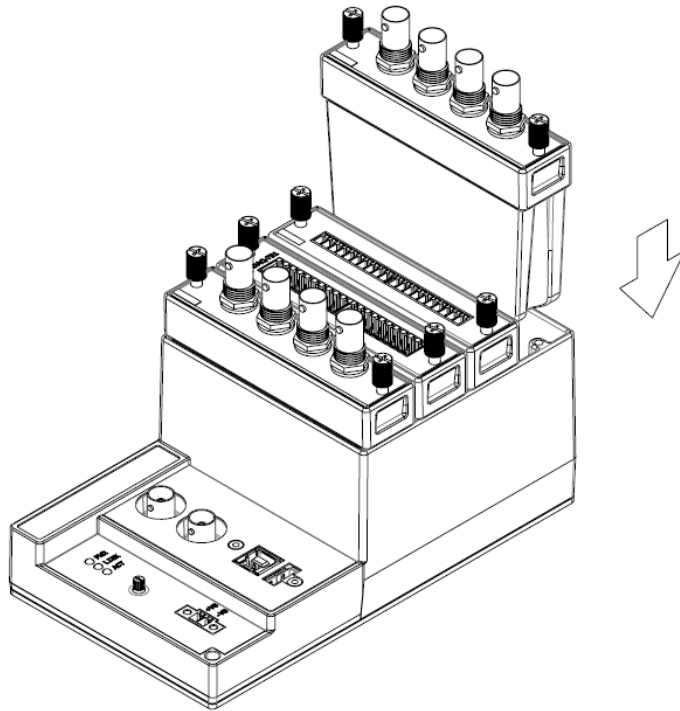


Figure 2.1 Installing iDAQ modules into the iDAQ chassis

2.2 Signal Connection and Pin Assignment

iDAQ-784 has four general-purpose 32-bit counter/timers and one frequency generator. The general-purpose counter/timers can be used for many measurement and pulse generation applications. The signal connection for each function are described in the following sections.

2.2.1 Pin Assignment

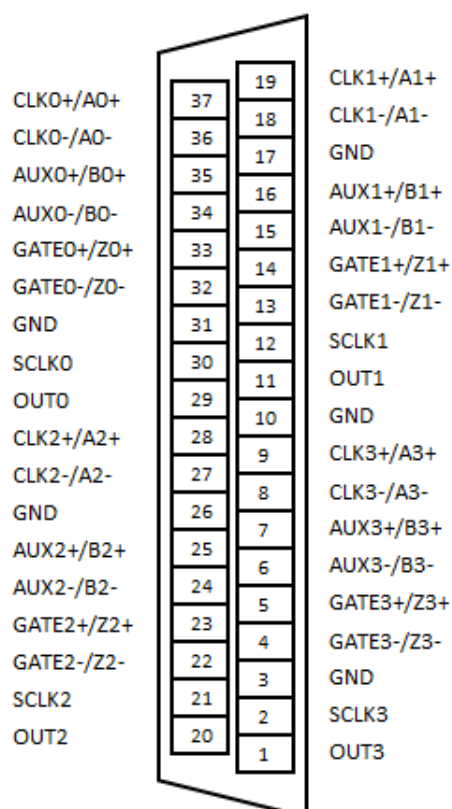


Figure 2.2 Pin assignment of iDAQ-784

Table 2.1: Description of each pin of iDAQ-784

Pin Name	Description
CLK _n +/ _A _n + <0...3>	Positive input of the clock input (general purpose counter) or signal A input (encoder counter) of counter channel n
CLK _n -/ _A _n - <0...3>	Negative input of the clock input (general purpose counter) or signal A input (encoder counter) of counter channel n
AUX _n +/ _B _n + <0...3>	Positive input of signal B input (encoder counter) of counter channel n
AUX _n -/ _B _n - <0...3>	Negative input of signal B input (encoder counter) of counter channel n
GATE _n +/ _Z _n + <0...3>	Positive input of gate input (general purpose counter) or signal Z input (encoder counter) of counter channel n
GATE _n -/ _Z _n - <0...3>	Negative input of gate input (general purpose counter) or signal Z input (encoder counter) of counter channel n
SCLK _n <0...3>	Sample clock input (general purpose counter) or (encoder counter) of counter channel n
OUT _n <0...3>	Output of counter channel n
GND	Ground

2.2.2 Event Counting

In event counting mode, the counter counts the number of edges of the input signal. It accepts both single end and differential connection. The signal connections are shown in the figure 2.3 for single ended and differential respectively. The gate can also be employed to enable or disable the counting,

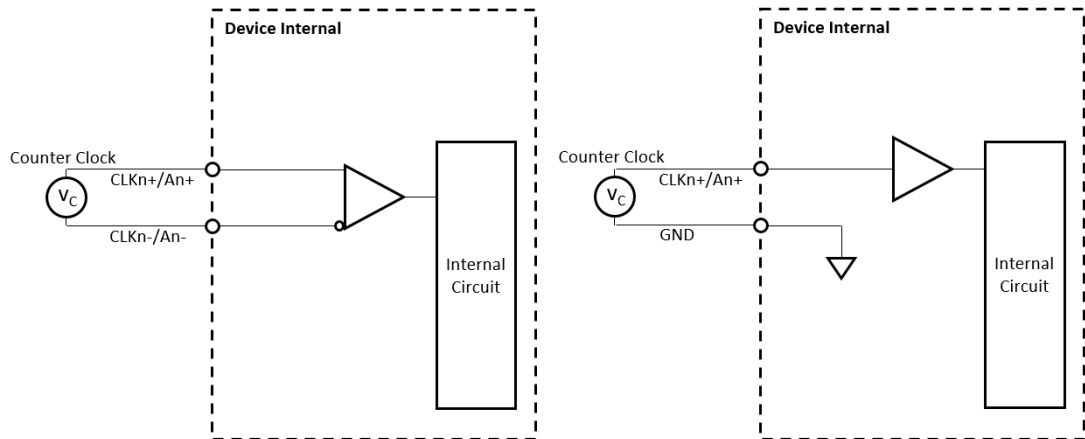


Figure 2.3 Event counting signal connection, differential (left), single end (right)

2.2.3 Frequency Measurement and Pulse Width Measurement

In frequency measurement and pulse width measurement modes, the iDAQ-784 measures the frequency of a periodic pulse train via the Gate/Z pins. It also accepts both single end and differential connection types. The signal connection is shown in Figure 2.4.

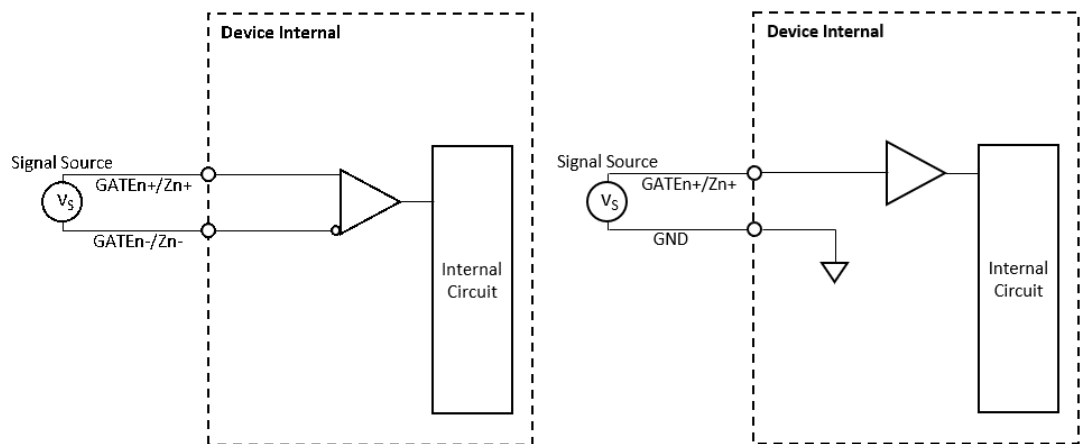


Figure 2.4 Frequency Measurement signal connection, differential (left), single end (right)

2.2.4 Position Measurement and Continue Compare

In position measurement mode, the position signal source is external encoders. There are three encoder types: Pulse-Direction (Signed Pulse), Two Pulse (CW/CCW), AB Phase (Quadrature). Alternatively, the function Continue Compare relies on setting the Compare Table/Interval to generate the pulse output/hardware interrupt when the configured counting is reached. The corresponded signal connection for each encoder type is described in Figure 2.5 and Table 2.2.

The A, B, and Z pins are corresponded encoder connection. The SCLK on the other hand, is used whenever users would like to employ the snap counting (refer to 3.4.9 for detail information) function. The OUT pin is the output pin of the compare function (refer to 3.5 for detail information).

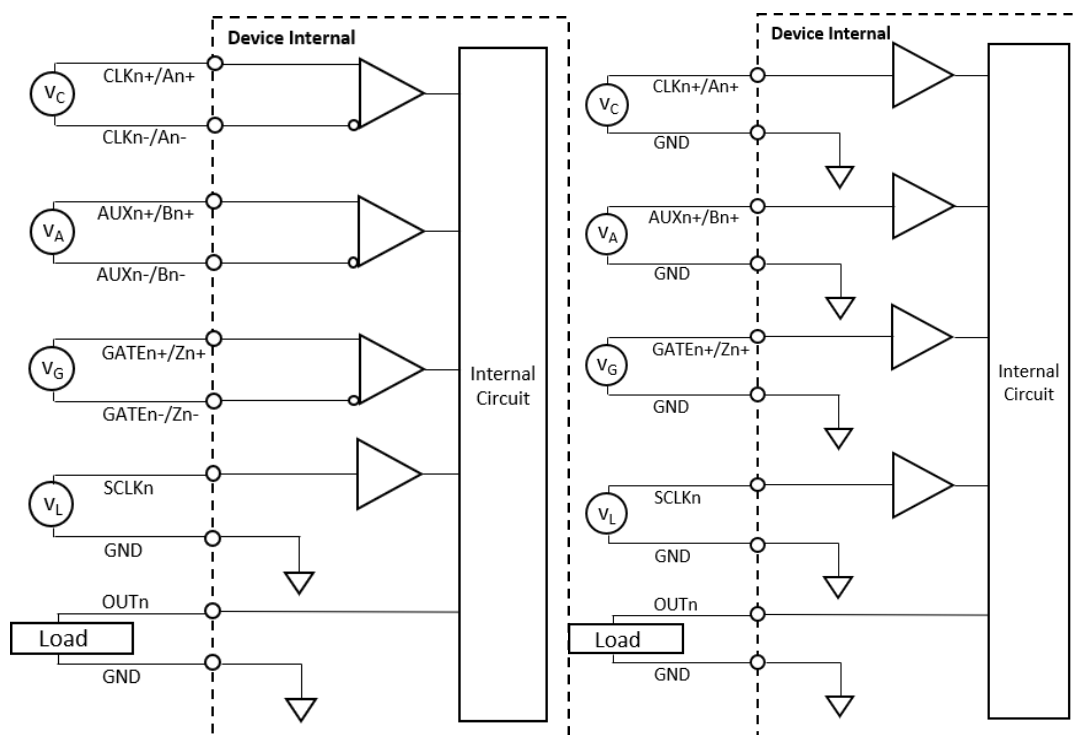


Figure 2.5 Signal Connection for Position Measurement and Continue Compare, (Left) Differential Encoder, (Right) Single-ended Encoder

Table 2.2: Encoder connection against different encoder types

Counter Pin	Encoder Types		
	Pulse-Direction (Signed Pulse)	Two-pulse (CW/CCW)	AB Phase (Quadrature)
CLKn/An	Clock	Up Counting	Signal A
AUXn/Bn	Direction	Down Counting	Signal B
GATEn/Zn	-	--	Signal Z
SCLKn		Counting Latching	
OUTn		Compare Output	

2.2.5 One-shot (Delayed Pulse Generation)

In one-shot mode, when an active edge of gate signal is detected, a pulse will be generated to the OUT pin after the specified number source clock counts. The pulse width is one period of source clock. The signal connection is shown in Figure 2.6.

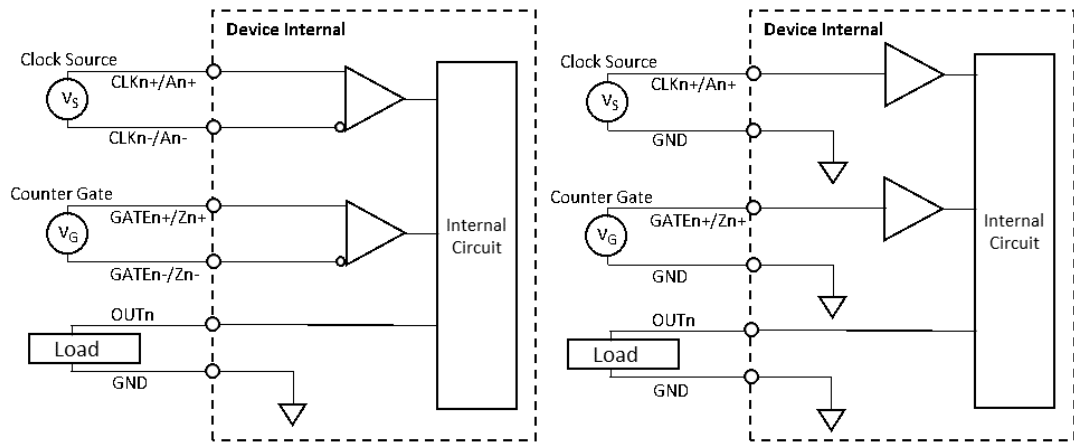


Figure 2.6 Signal Connection for One Shot (delayed pulse generation), (Left) Differential signal & gate source, (Right) Single-ended signal & gate source

2.2.6 Timer Pulse (with Interrupt) and Pulse Width Modulation

The pulse output function includes Timer Pulse and Pulse Width Modulation. They send the continuous pulses on specified frequency and duty cycle via OUT pin. They can also be controlled by Gate pin. The corresponded signal connection is shown in Figure 2.7.

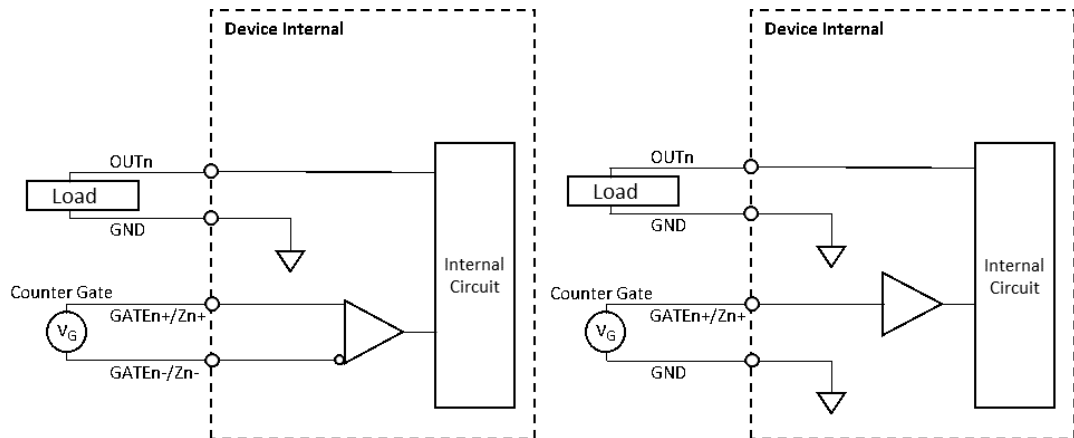


Figure 2.7 Signal Connection for Timer Pulse and Pulse Width Modulation, (Left) Differential gate, (Right) Single-ended gate

Chapter 3

Function Details

3.1 Event Counting

In event counting mode, the counter counts the number of edges the counter clock signal generates. It can be configured as rising edge active or falling edge active, as shown in Figure 3.1 and Figure 3.2, respectively.

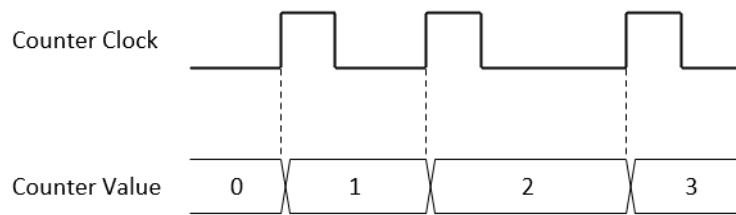


Figure 3.1 Rising edge event counting

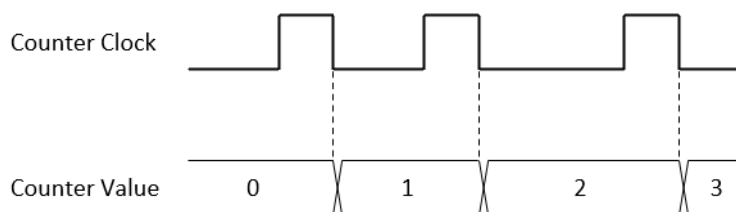


Figure 3.2 Falling edge event counting

Counting may be temporarily paused by the counter gate signal as shown in Figure 3.3.

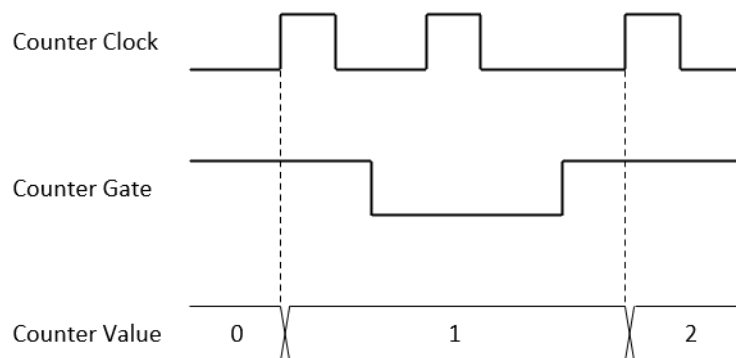


Figure 3.3 Event counting with pause gate

3.1.1 Instant (Software-Timed) Event Counting

With instant event counting, the software controls the rate and time of reading counter value, which is thus also called software-timed event counting. Whenever the software sends a read command, the current value of the counter is returned as shown in Figure 3.4.

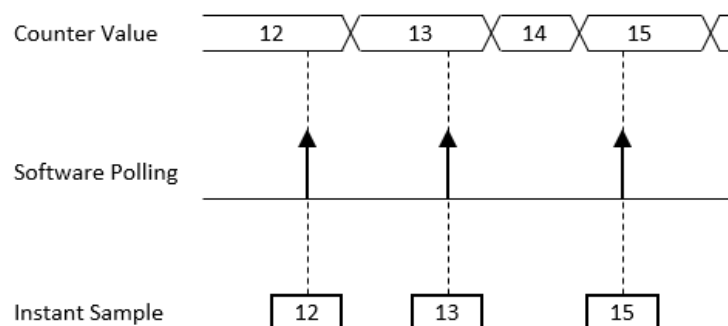


Figure 3.4 Instant (software-timed) event counting

The advantage of instant event counting is low latency. It is typically used for reading a single sample of counter value.

Note: In software-timed value reading, the response time is system resource dependent. For a stable data reading interval, please use buffered function instead.

3.1.2 Buffered (Hardware-Timed) Event Counting

With buffered event counting, a hardware signal called sample clock controls the rate and time of reading counter value as shown in Figure 3.5. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

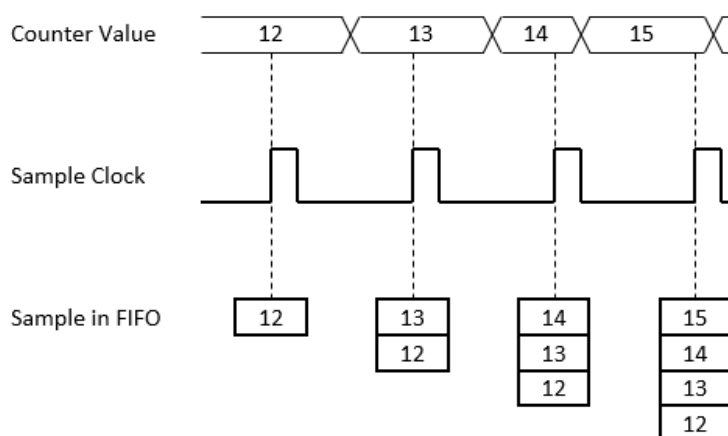


Figure 3.5 Buffered (hardware-timed) event counting

The read samples are first accumulated in the onboard first-in-first-out (FIFO) memory, and then moved to the buffer in the PC by a direct memory access (DMA) engine. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the memory. Because the data is moved in large blocks instead of one point at a time, buffered event counting typically allow much higher transfer rates. Buffered event counting is also called hardware-timed event counting.

The advantages of buffered event counting over instant event counting include:

- The sample rate can be much higher.
- The time of sample is deterministic.

3.2 Frequency Measurement

In frequency measurement mode, the frequency of the counter clock signal is measured by one of the two measuring methods: Period inversion or counting number of pulses in fixed duration. There's also an option auto-adaptive for relying on the system itself to decide the mode according to the input signal type.

3.2.1 Period Inversion

In this method, the period of the counter clock signal is firstly measured by an internal high frequency clock. The frequency of the signal is then calculated by inverting the period value. This is shown in Figure 3.6 and by the following equation.

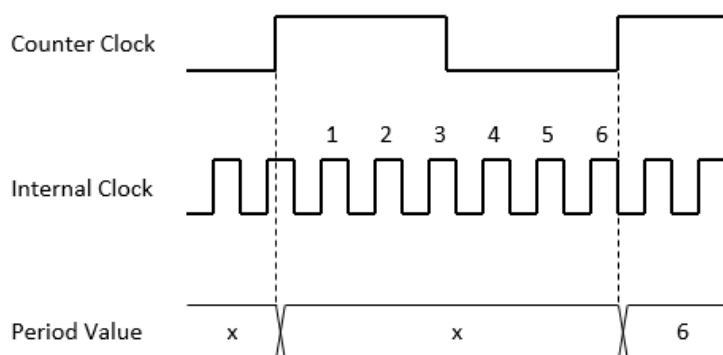


Figure 3.6 Frequency measurement by period inversion

$$Frequency = \frac{1}{Period} = \frac{1}{InternalClockCount \times InternalClockPeriod}$$

This method is suitable if the counter clock signal frequency is much smaller (< 0.1%) than the internal clock frequency. Measuring accuracy degrades as the counter clock signal frequency increases.

3.2.2 Counting Number of Pulses in Fixed Duration

In this method, the pulse number of the counter clock signal is measured in a fixed time duration. The frequency of the signal is then calculated by dividing this number by the time duration. This is shown in Figure 3.7 and by the following equation.

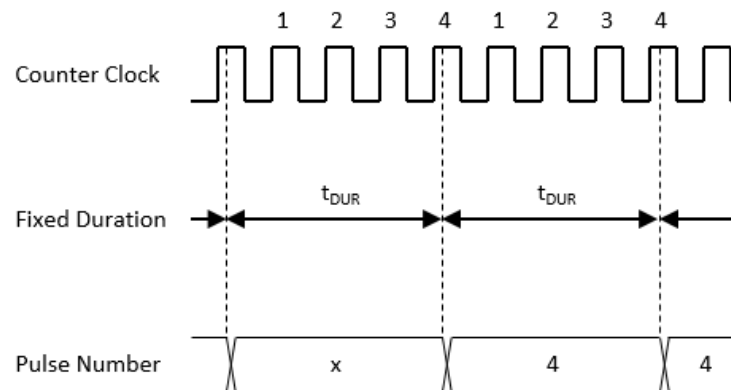


Figure 3.7 Frequency measurement by counting number of pulses in fixed duration

$$Frequency = \frac{PulseNumber}{t_{DUR}}$$

For counter clock signal frequency higher than that specified in the previous section, this method gives a more accurate result.

3.2.3 Measurement Time-up

During the measurement, the signal source may stop sending pulses for somewhat reason. In this context, the frequency should be 0 Hz. The counter should then be aware that there're no longer updates from the signal source, and return the measured frequency to 0 Hz. A setting Time-up is to determine how long should the counter be waited before returning 0 Hz. For example, when setting 1 second for timeup, the counter would wait for 1 second after it receives the last pulse, and return 0 Hz when 1 second is reached and there's not any pulse counted anymore during the period.

3.3 Pulse Width Measurement

In pulse width measurement mode, both the high period and the low period of the counter clock signal are measured. The measured values are updated when a pulse is completed. This is shown in Figure 3.8.

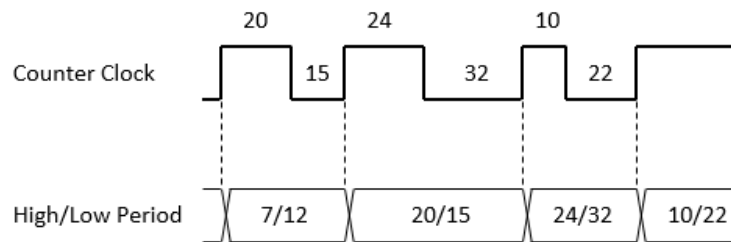


Figure 3.8 Pulse width measurement

3.3.1 Instant (Software-Timed) Pulse Width Measurement

With instant pulse width measurement, the software controls the rate and time of reading counter value, which is thus also called software-timed pulse width measurement. Whenever the software sends a read command, the current value of the counter is returned as shown in Figure 3.9.

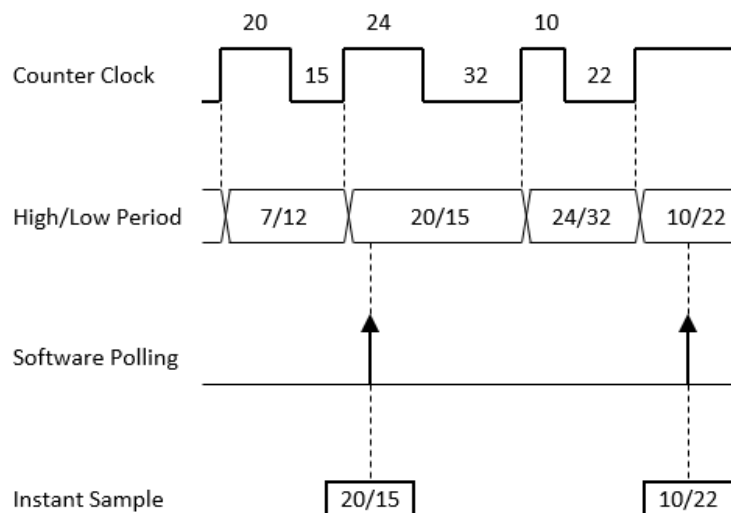


Figure 3.9 Instant (software-timed) pulse width measurement

The advantage of instant pulse width measurement is low latency. It is typically used for reading a single sample of counter value.

Note: In software-timed value reading, the response time is system resource dependent. For a stable data reading interval, please use buffered function instead.

3.3.2 Sample Clock Buffered (Hardware-Timed) Pulse Width Measurement

With sample clock buffered pulse width measurement, a hardware signal called sample clock controls the rate and time of reading counter value as shown in Figure 3.10. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

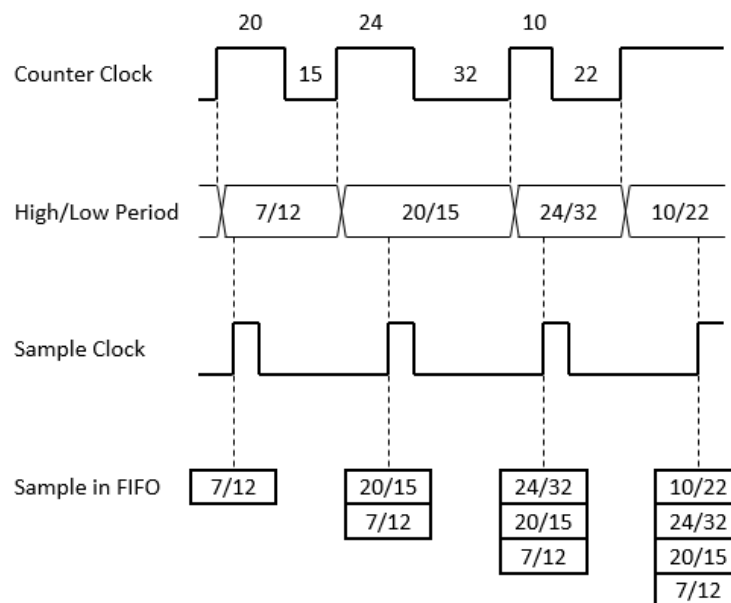


Figure 3.10 Sample clock buffered (hardware-timed) pulse width measurement

The read samples are first accumulated in the onboard first-in-first-out (FIFO) memory, and then moved to the buffer in the PC by a direct memory access (DMA) engine. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the application memory. Because the data is moved in large blocks instead of one point at a time, buffered pulse width measurement typically allow much higher transfer rates. Buffered pulse width measurement is also called hardware-timed pulse width measurement.

The advantages of buffered pulse width measurement over instant pulse width measurement include:

- The sample rate can be much higher.
- The time of sample is deterministic.

3.3.3 Measurement Time-up

During the measurement, the signal source may stop sending pulses for somewhat reason. In this context, the high and low period should be both 0. The counter should then be aware that there are no longer updates from the signal source, and return the measured high and low period as 0. A setting Time-up is to determine how long should the counter be waited before returning 0. For example, when setting 1 second for timeup, the counter would wait for 1 second after it receives the last pulse, and return 0 when 1 second is reached and there's not any pulse counted anymore during the period.

3.4 Position Measurement

In position measurement mode, the condition for increasing or decreasing of the counter value depends on the input mode, they are Quadrature (AB phase), Two-pulse (CW/CCW), and Pulse-direction (Signed Pulse) respectively.

3.4.1 Quadrature x1 Mode

In quadrature x1 mode, if counter A signal leads counter B signal by 90 degrees, the counter value is increased by 1 for each pulse period. If counter B signal leads counter A signal by 90 degrees, the counter value is decreased by 1 for each pulse period. They are shown in Figure 3.11 and Figure 3.12, respectively.

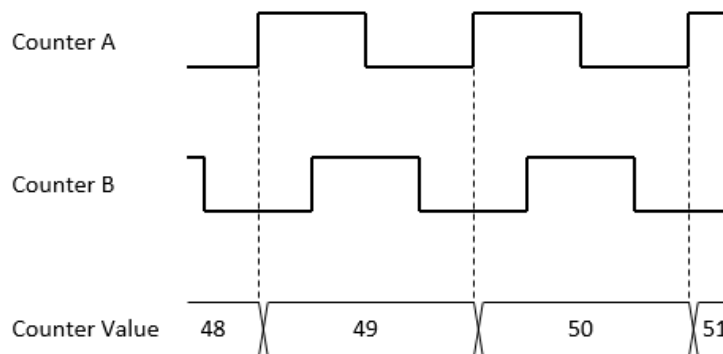


Figure 3.11 Quadrature x1 mode, counter A leads counter B

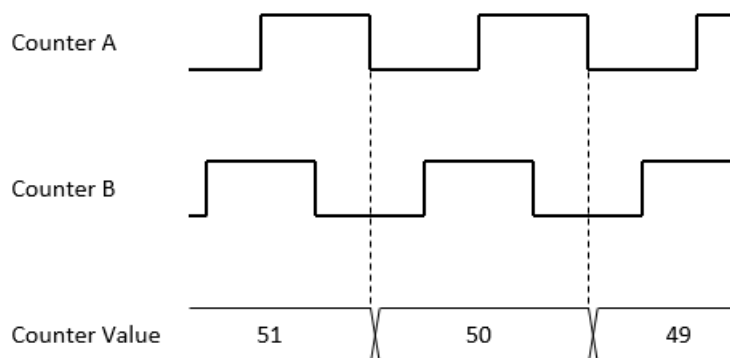


Figure 3.12 Quadrature x1 mode, counter B leads counter A

3.4.2 Quadrature x2 Mode

In quadrature x2 mode, if counter A signal leads counter B signal by 90 degrees, the counter value is increased by 2 for each pulse period. If counter B signal leads counter A signal by 90 degrees, the counter value is decrease by 2 for each pulse period. They are shown in Figure 3.13 and Figure 3.14, respectively.

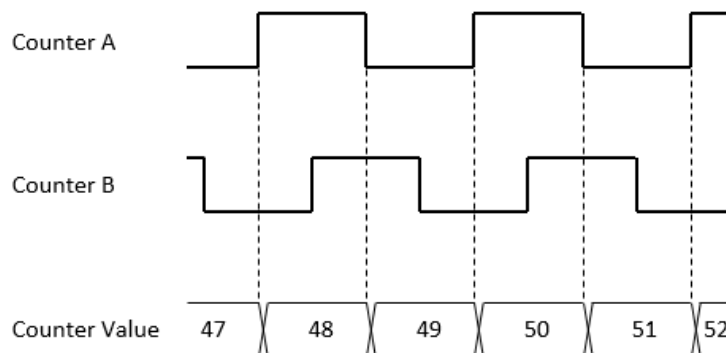


Figure 3.13 Quadrature x2 mode, counter A leads counter B.

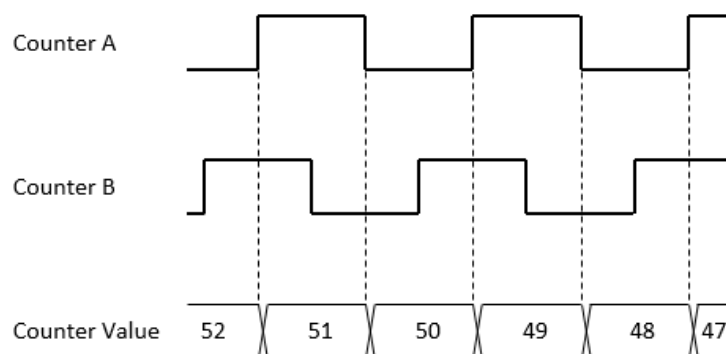


Figure 3.14 Quadrature x2 mode, counter B leads counter A

3.4.3 Quadrature x4 Mode

In quadrature x4 mode, if counter A signal leads counter B signal by 90 degrees, the counter value is increased by 4 for each pulse period. If counter B signal leads counter A signal by 90 degrees, the counter value is decrease by 4 for each pulse period. They are shown in Figure 3.15 and Figure 3.16, respectively.

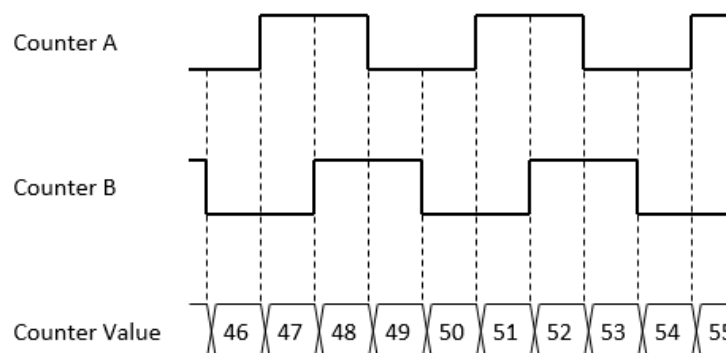


Figure 3.15 Quadrature x4 mode, counter A leads counter B

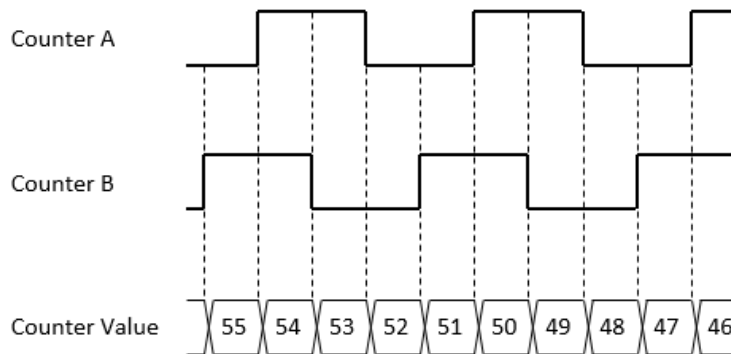


Figure 3.16 Quadrature x4 mode, counter B leads counter A

3.4.4 Two Pulse (CW/CCW) Mode

In two pulse (or clockwise/counter-clockwise) mode, the counter value is increased by 1 for each pulse of counter A signal, and is decreased by 1 for each pulse of counter B signal. This is shown in Figure 3.17.

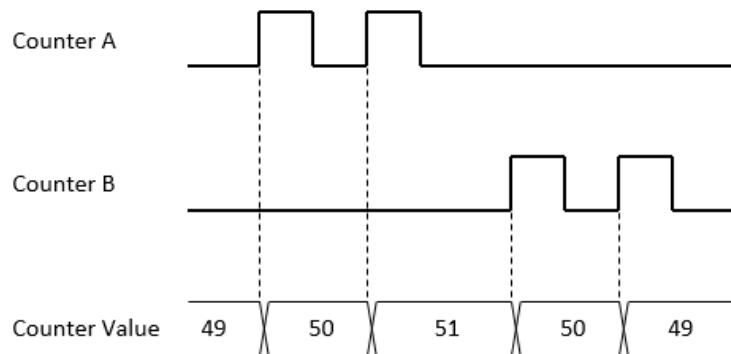


Figure 3.17 Two pulse (clockwise/counter-clockwise) mode.

3.4.5 Pulse-direction (Signed Pulse) Mode

In signed pulse (or pulse/direction) mode, the counting direction is controlled by counter B signal. The counter value is increased by 1 for each pulse of counter A signal when counter B signal is low. It is decreased by 1 for each pulse of counter A signal when counter B signal is high. This is shown in Figure 3.18.

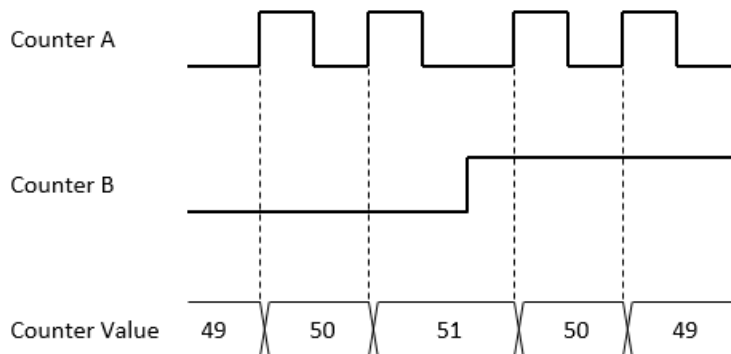


Figure 3.18 Signed pulse (pulse/direction) mode.

3.4.6 Position Reset

In position measurement, the counter value can be reset to zero either by the software or by the counter Z signal. Figure 3.19 shows an example of reset by counter Z signal.

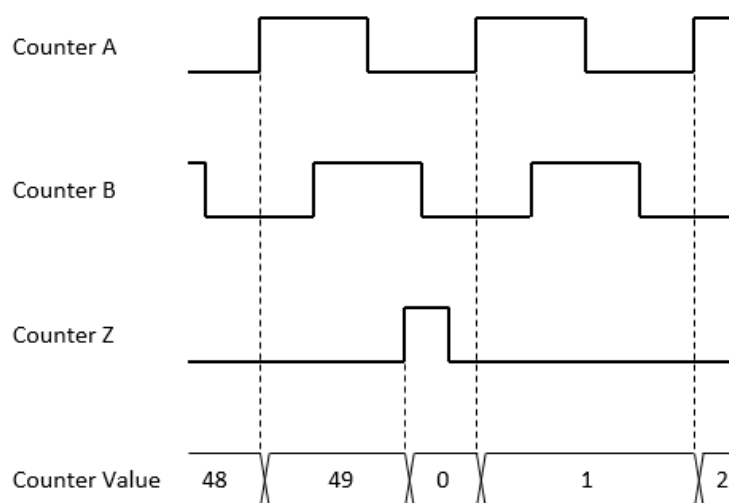


Figure 3.19 Position reset to 0 by counter Z signal

3.4.7 Instant (Software-Timed) Position Measurement

With instant position measurement, the software controls the rate and time of reading counter value, which is thus also called software-timed position measurement. Whenever the software sends a read command, the current value of the counter is returned as shown in Figure 3.20.

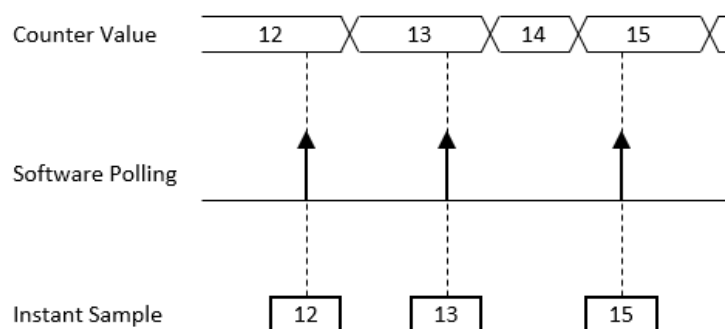


Figure 3.20 Instant (software-timed) position measurement

The advantage of instant position measurement is low latency. It is typically used for reading a single sample of counter value.

Note!



In software-timed value reading, the response time is system resource dependent. For a stable data reading interval, please use buffered function instead.

3.4.8 Buffered (Hardware-Timed) Position Measurement

With buffered position measurement, a hardware signal called sample clock controls the rate and time of reading counter value as shown in Figure 3.21. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

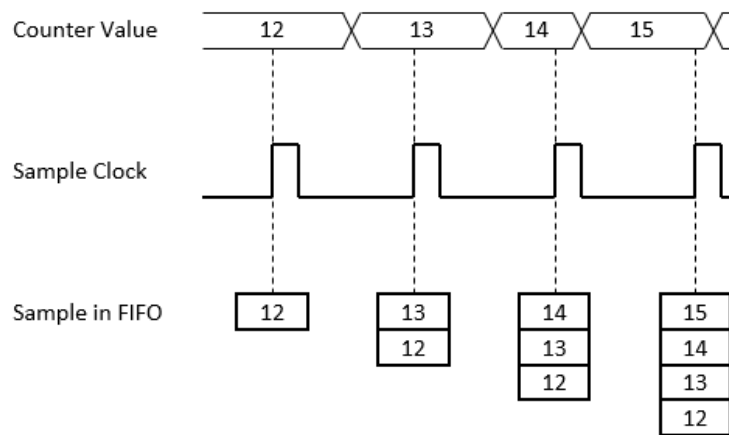


Figure 3.21 Buffered (hardware-timed) position measurement.

The read samples are first accumulated in the onboard first-in-first-out (FIFO) memory, and then moved to the buffer in the PC by a direct memory access (DMA) engine. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the application memory. Because the data is moved in large blocks instead of one point at a time, buffered position measurement typically allow much higher transfer rates. Buffered position measurement is also called hardware-timed position measurement.

The advantages of buffered position measurement over instant position measurement include:

- The sample rate can be much higher.
- The time of sample is deterministic.

3.4.9 Snap Counting

When the counter snapping function is started and receiving the trigger from SCLK pin, a software event would be generated, and the driver will scan all the counters and take a snapshot to these channels. The scanned data will be transferred to the user by the corresponding counter event.

3.5 Position Comparison

An output pulse can be generated at the counter output terminal when the position value matches the specified compare value. This is shown in Figure 3.22. The width of the output pulse is configurable.

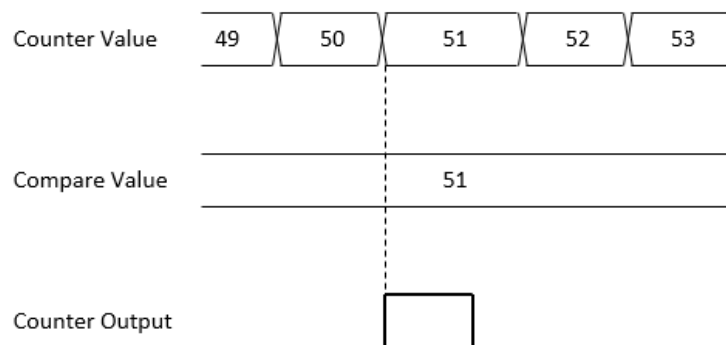


Figure 3.22 Position comparison

3.5.1 Instant Position Comparison

With instant position comparison, software controls the update of the compare value. A software interrupt will be generated when a compare match occurs, and the software can update the compare value accordingly. This is shown in Figure 3.23.

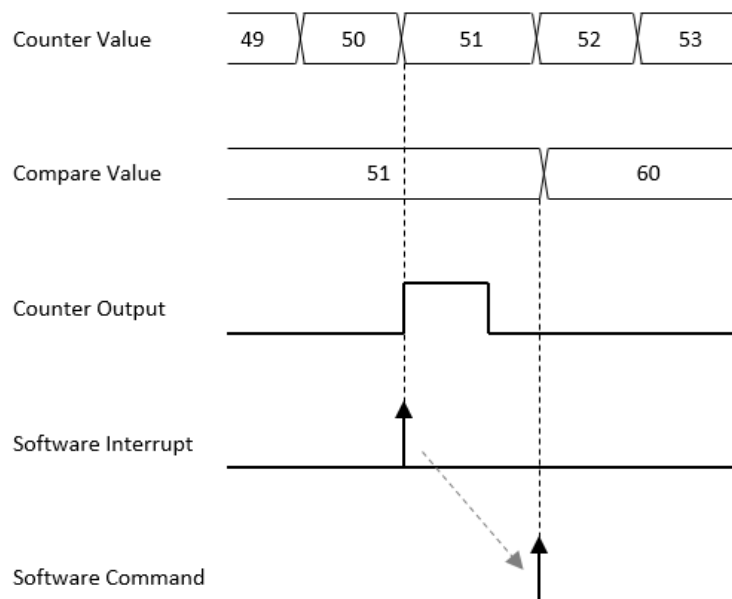


Figure 3.23 Instant position comparison

The advantage of instant position comparison is that the next compare value can be decided on the fly.

Note: In software-timed value reading, the response time is system resource dependent. For a stable data reading interval, please use buffered function instead.

3.5.2 Buffered Position Comparison (Pre-loaded Table)

With buffered position comparison, the compare values are pre-programmed by the software and then stored in the on-board FIFO. When a value match occurs, the next compare value will be automatically loaded by the hardware as shown in Figure 3.24.

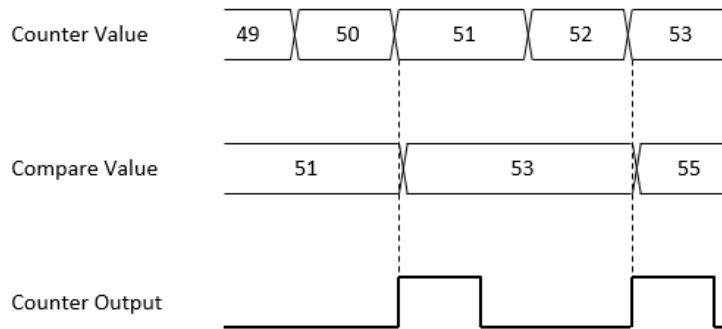
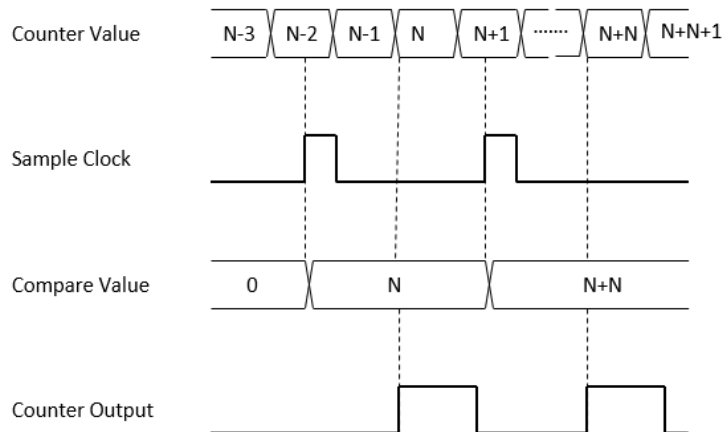


Figure 3.24 Buffered position comparison

Due to the low latency of hardware operation, buffered position comparison support much higher update rate of the compare value over instant position comparison.

3.5.3 Buffered Position Comparison (Fixed Interval)

The position comparison can also be set using a fixed interval. With fixed interval N set, the counter output would be generated at every N encoder steps.



3.6 One-Shot (Delayed Pulse Generation)

In one-shot mode, when an active edge of gate signal is detected, a pulse will be generated after the specified number source clock counts. The pulse width is one period of source clock. Figure 3.26 shows an example of high-pulse, 5-clock delay one-shot output.

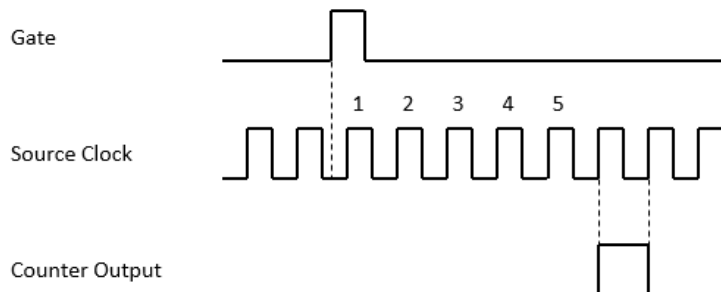


Figure 3.25 One-shot operation

3.7 Timer/Pulse (with Interrupt)

In timer/pulse mode, continuous pulses with specified frequency are generated at counter output terminal, and an interrupt is also generated with each pulse as shown in Figure 3.27.

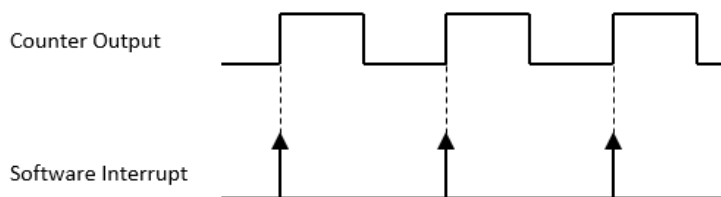


Figure 3.26 Pulse output and timer interrupt

The output can be gated. If counter gate is in active level, pulses are output normally. On the other hand, if counter gate is in inactive level, output is disabled. Figure 3.28 shows an example of active high gate.

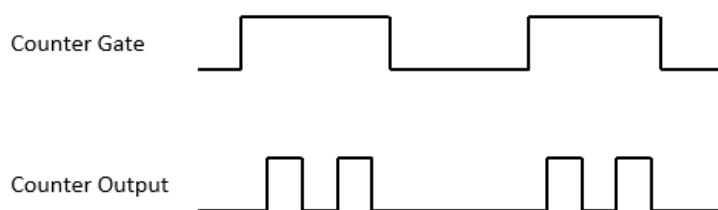


Figure 3.27 Gated timer/pulse output

3.7.1 Static (Software-Timed) Timer/Pulse

With static timer/pulse, the software controls the time of updating output pulse frequency, which is thus also called software-timed timer/pulse. Whenever the software sends an update command, the frequency of output pulse is updated to the specified value after current pulse is completed as shown in Figure 3.29.

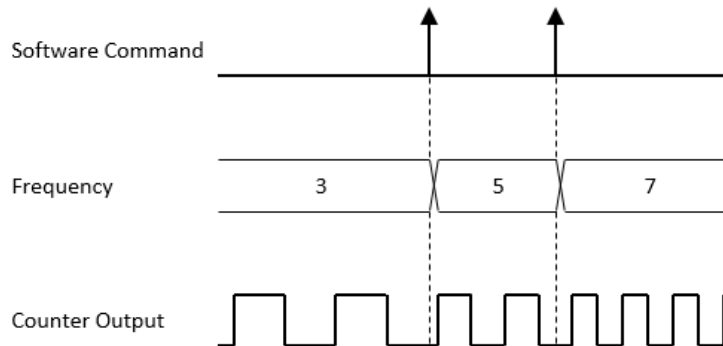


Figure 3.28 Static (software-timed) timer/pulse

Note: In software-timed value reading, the response time is system resource dependent. For a stable data reading interval, please use buffered function instead.

3.7.2 Buffered (Hardware-Timed) Timer/Pulse

With buffered timer/pulse, a hardware signal called sample clock controls the time of updating output pulse frequency as shown in Figure 3.30. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

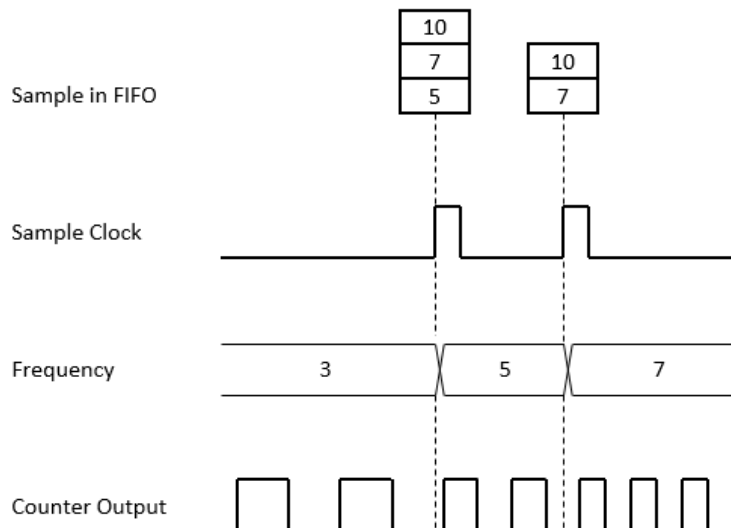


Figure 3.29 Buffered (hardware-timed) timer/pulse

The samples to be updated are first written to the onboard first-in-first-out (FIFO) memory by software. Each time a rising edge of sample clock is detected, the first sample in the FIFO is used to update the output pulse frequency, and then the sample is discarded. Buffered timer/pulse is also called hardware-timed timer/pulse.

The advantages of buffered timer/pulse over static timer/pulse include:

- The time of sample is deterministic.
- The time of sample can be controlled by an external signal.

3.8 Pulse Width Modulation (PWM Output)

In pulse width modulation (PWM) output mode, a pulse waveform with specified high period (t_{HIGH}) and low period (t_{LOW}) is output at counter output terminal as shown in Figure 3.31.

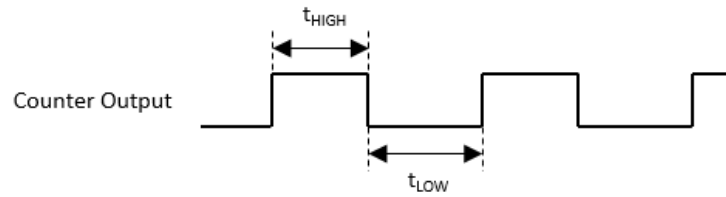


Figure 3.30 Pulse width modulation output

The number of pulses generated can be finite or infinite. For finite pulse generation, the counter output starts generating pulses when armed, and automatically stops after the specified number of pulses has completed. The counter can be re-armed after the previous generation is completed. This is shown in Figure 3.32.

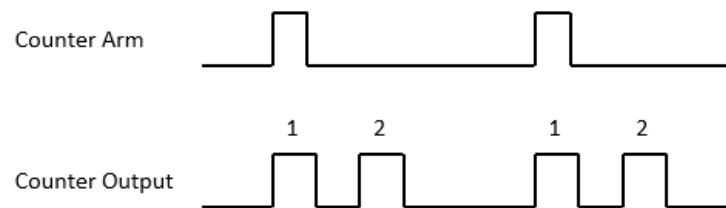


Figure 3.31 Finite pulse generation

For infinite pulse generation, the counter output starts generating pulses when armed and continues until stopped by software. This is shown in Figure 3.33.

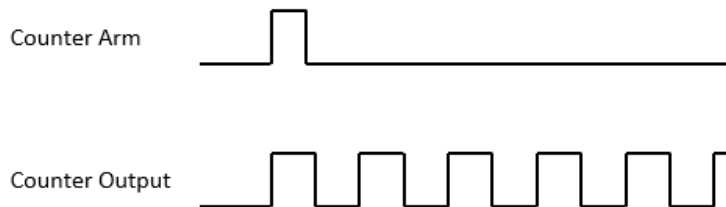


Figure 3.32 Infinite pulse generation

The output can be gated. If counter gate is high, pulses are output normally. On the other hand, if counter gate is low, output is disabled. This is shown in Figure 3.34.

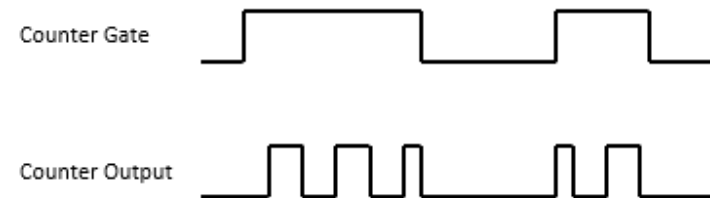


Figure 3.33 Gated pulse width modulation output

3.8.1 Static (Software-Timed) PWM Output

With static PWM output, the software controls the time of updating output pulse width, which is thus also called software-timed timer/pulse. Whenever the software sends an update command, the width of output pulse is updated to the specified value after current pulse is completed as shown in Figure 3.35.

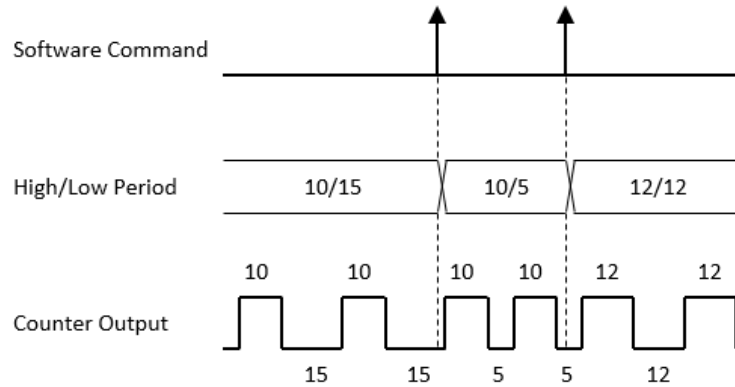


Figure 3.34 Static (software-timed) timer/pulse

Note! In software-timed value reading, the response time is system resource dependent. For a stable data reading interval, please use buffered function instead.



3.8.2 Buffered (Hardware-Timed) PWM Output

With sample clock buffered PWM output, a hardware signal called sample clock controls the time of updating output pulse width as shown in Figure 3.36. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

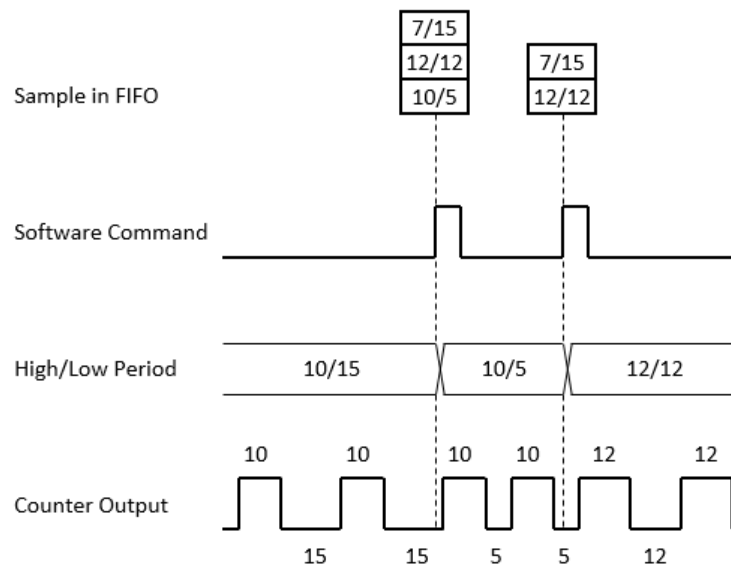


Figure 3.35 Sample clock buffered pulse width modulation output

The samples to be updated are first written to the onboard first-in-first-out (FIFO) memory by software. Each time a rising edge of sample clock is detected, the first sample in the FIFO is used to update the output pulse width, and then the sample is discarded. Buffered PWM output is also called hardware-timed PWM output.

The advantages of buffered PWM output over static PWM output include:

- The time of sample is deterministic.
- The time of sample can be controlled by an external signal.

3.9 Device Description and Configuration

The Device Description is used to differentiate the modules in the iDAQ system. It's given following a naming rule of combining chassis ID, model name and slot number. You can change the description in Navigator, or just leave it as default. The description is used in your own program, in order to get control or device handler from the device.

Appendix **A**

Specifications

A.1 Counter

- Channels: 4
- Resolution: 32 bits
- Max. Input Frequency: 10 MHz
- Max. Output Frequency: 10 MHz
- Digital Filter: 40 ns ~ 84 ms
- Supported Functions: Event Counter, Position Measurement, Position Compare, Pulse Width Measurement, One Shot, Timer/Pulse, Pulse Width Modulation

Measurement Functions

- Event Counting
 - Input frequency: 10 MHz max.
 - Clock polarity: Rising edge or falling edge, software configurable
 - Gate function: Enabled or disabled, software configurable
 - Gate polarity: High active or low active, software configurable
 - Measuring type: Instant or sample clock buffered, software configurable
- Frequency Measurement
 - Measuring method: Counting pulse by system time, period inverse, or auto adaptive, software configurable
 - Input frequency: 0.1 Hz ~ 10 MHz
 - Accuracy: 0.1%
 - Measuring type: Instant or sample clock buffered, software configurable
- Pulse Width Measurement
 - Pulse width range: 100 ns ~ 10 s
 - Pulse width resolution: 20 ns
 - Accuracy: 50 ppm of width + 20 ns
 - Measuring type: Instant or sample clock buffered, software configurable
- Position Measurement
 - Input frequency: 10 MHz max.
 - Measuring mode: Quadrature (A/B phase) x1, x2, x4, two-pulse (clockwise/counter-clockwise), pulse-direction (signed-pulse)
 - Counter reload by Z signal: Enabled or disabled, software configurable
 - Measuring type: Instant or sample clock buffered, software configurable

Output Functions

- One Shot (Delayed Pulse Generation)
 - Internal clock source frequency: 50 MHz
 - Internal clock source accuracy: 50 ppm
 - External clock source frequency: 10 MHz max.
 - Delay count: 1 ~ 4,294,967,295
 - Gate source: External
 - Gate polarity: Rising edge or falling edge, software configurable
 - Output signal type: Positive pulse or negative pulse, software configurable
 - Generation type: Static
- Timer/pulse
 - Timebase clock frequency: 50 MHz
 - Timebase clock accuracy: 50 ppm

- Output frequency: 0.1 Hz ~ 10 MHz
- Gate function: Enabled or disabled, software configurable
- Gate polarity: High active or low active, software configurable
- Interrupt generation: Enabled or disabled, software configurable
- Generation type: Static or sample clock buffered, software configurable
- Pulse Width Modulation
 - Timebase clock frequency: 50 MHz
 - Timebase clock accuracy: 50 ppm
 - Pulse width: 100 ns ~ 1 s
 - Pulse width resolution: 20 ns
 - Number of pulses: 1 ~ 4,294,967,295 or infinite, software configurable
 - Gate function: Enabled or disabled, software configurable
 - Gate polarity: High active or low active, software configurable
 - Generation type: Static, implicit buffered, or sample clock buffered, software configurable
- Position Compare
 - Compare value: Instant, buffered, software configurable
 - Output signal type: Positive pulse or negative pulse, software configurable
 - Output Pulse width: 100 ns ~ 1 s, software configurable

A.2 Electric Properties

Table A.1: Electric Properties

Properties	CLK (A)	AUX (B)	GATE (Z)	SCLK	OUT	
Direction	Input			Input	Output	
Compatibility	-12 V ~ 12 V			5V TTL	5V TTL	
Voltage Range	Single End	High: 2.8V min. Low: 0.8V max. (Positive to GND)		High: 2.8V min. Low: 0.8V max.	High: 4.0 V min. @ 2mA source/5.2V max. Low: 0.4 V max. @ 2mA sink.	
	Differential	High: 0.5V min. Low: -0.5V max. (Positive to Negative)		--	--	
Driving Capability	--			--	8 mA max.	
Input Common-mode Voltage Range	--15 V ~ 15 V			--	--	
Input Protection Voltage	-25 V ~ 25 V			--	--	
Isolation Protection	2500 V _{DC}			--	--	
Pull-up/down resistor	Pull-up 10 kΩ			--	--	
Debounce Filter	40 ns ~ 84 ms, software configurable			--	--	
Minimum Width				100 ns		
Counter Functions	Event Counter	v		v		
	Position Measurement	v	v	v	v	
	Frequency Measurement			v		
	Position Compare	v	v	v	v	v
	Pulse Width Measurement			v		
	One Shot	v		v		v
	Timer/Pulse	v		v		
	Pulse Width Modulation			v		v

A.3 Buffered Acquisition Properties

- Internal data buffer (FIFO) size
 - For measurement functions: 1,024 samples for each counter
 - For output functions: 1,024 samples for each counter
- Sample clock rate: 200 kHz max.
- Sample clock source: From chassis (all channels share the same clock signal) or external (each channel uses independent clock signal)

A.4 Trigger

- Number of triggers: 2 max., selectable via software
- Trigger action: Start, delay to start, stop, or delay to stop
- Trigger delay range: 0 ~ 16,777,215 samples
- Sample number: 0 ~ 16,777,215 samples

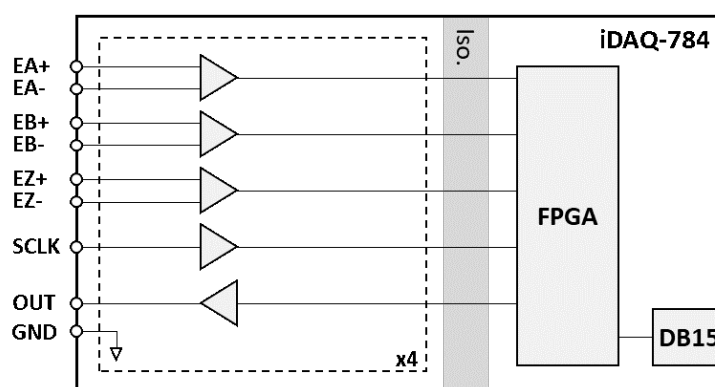
A.5 Power Consumption

- Typical 0.95W
- Maximum 1.07W

A.6 General

- Form factor: iDAQ Module
- Dimension: 100 x 80 x 25 mm (3.94 x 3.15 x 0.98 in.)
- Weight: 175 g
- I/O connector: 37-pin D-SUB
- Operating temperature: -40 °C to 70 °C (-40 °F to 158 °F)
- Storage temperature: -40 °C to 85 °C (-40 °F to 185 °F)
- Operating humidity: Up to 90% RH, non-condensing
- Storage humidity: Up to 95% RH, non-condensing
- Vibration: 5Grms, Random Vibration
- Shock: 30G
- Indoor use only.

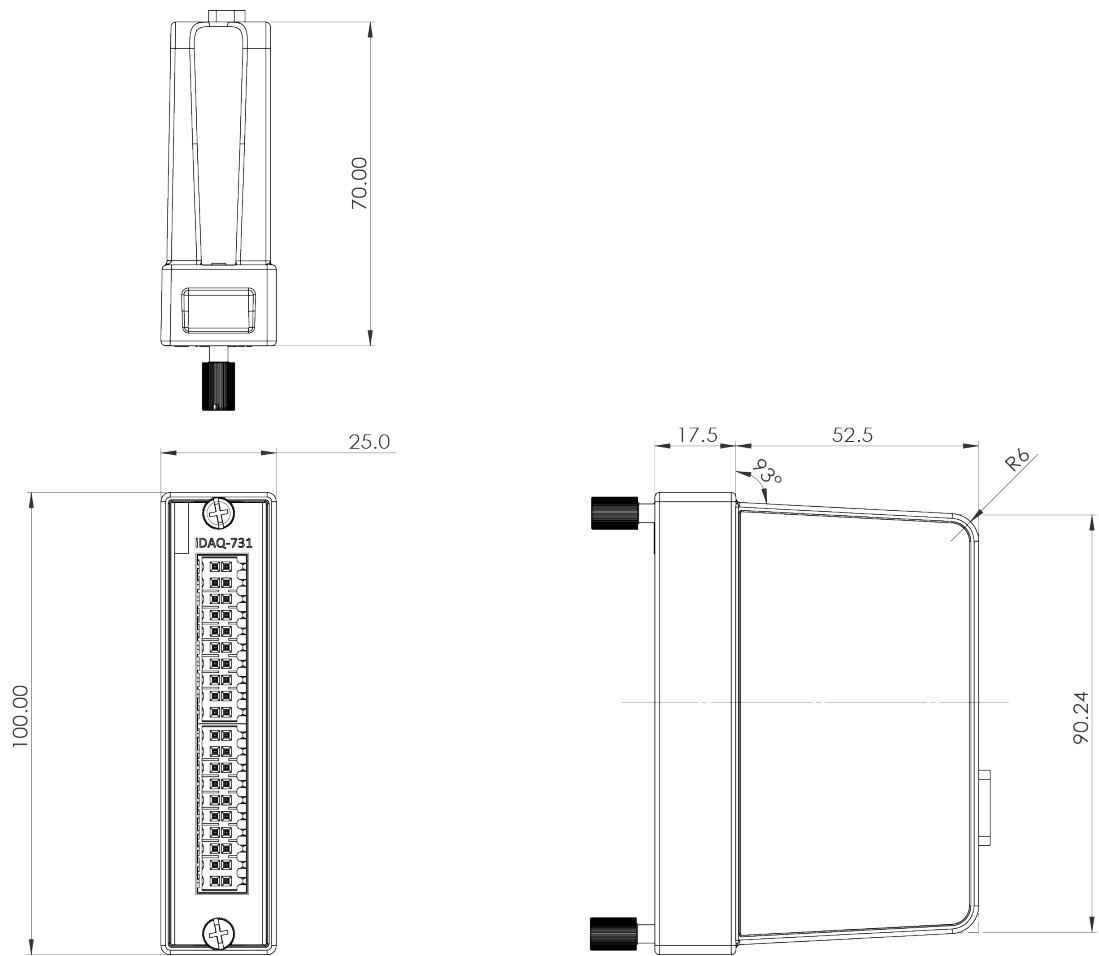
A.7 Function Block



Appendix **B**

System Dimensions

B.1 iDAQ Modules



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Please verify specifications before quoting. This guide is intended for reference purposes only.

All product specifications are subject to change without notice.

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